

Claims

- 1 1. Drive circuit for driving an output stage of a device for noise suppression, in
2 particular in a motor vehicle, comprising:
 - 3 - a first input for coupling in an unmodulated first clock signal of a first
4 frequency,
 - 5 - a second input for coupling in a PWM-modulated second clock signal of a
6 second, lower frequency,
 - 7 - a modulator circuit which from the first clock signal generates a PWM-
8 modulated third clock signal of the first frequency which can be tapped at the
9 PWM output of the drive circuit, and
 - 10 - a regulating circuit which regulates the pulse width of the third clock signal
11 until the sum of the pulse duty factors of the second clock signal and of the
12 inverted third clock signal is 100%.
- 1 2. Drive circuit according to Claim 1, wherein the regulating circuit has an
2 addresser which generates a first regulating signal from the sum of the second clock
3 signal and of the inverted third clock signal.
- 1 3. Drive circuit according to Claim 2, wherein the addresser has a first voltage
2 divider whose resistors have the same conductance.
- 1 4. Drive circuit according to Claim 2, wherein the regulating circuit has a first
2 comparator which generates the first regulating signal for driving the modulator circuit
3 as a function of a difference between a reference potential and a summation signal
4 generated by the addresser.
- 1 5. Drive circuit according to Claim 4, wherein for generating the reference
2 potential a second voltage divider is provided which is located between terminals of a
3 supply voltage source.

- 1 6. Drive circuit according to Claim 1, wherein the regulating circuit is designed as
- 2 a PID regulator and/or as an I regulator.

- 1 7. Drive circuit according to Claim 1, wherein the modulator circuit has a NAND
- 2 gate, a downstream ramp generator, second comparator, and flip-flop.

- 1 8. Drive circuit according to Claim 7, wherein the ramp generator has a
- 2 switchable current source and an integration capacitor for generating a ramp voltage.

- 1 9. Drive circuit according to Claim 7, wherein the second comparator is
- 2 connected on the input side to the output of the ramp generator and to the output of the
- 3 regulating circuit, with the second comparator comparing the ramp voltage with the
- 4 first regulating signal and, as a function of this, generating a trigger signal for
- 5 triggering the flip-flop.

- 1 10. Drive circuit according to Claim 7, wherein the flip-flop is connected on the
- 2 input side to the first input and to the output of the second comparator, with the flip-
- 3 flop making the third clock signal and a clock signal inverted with respect to this
- 4 available at the output as a function of the trigger signal and of the first clock signal.

- 1 11. Drive circuit according to Claim 1, wherein the drive circuit is a component
- 2 part of a program-controlled unit, in particular of a microcontroller or microprocessor.

1 12. Devices for electronic noise suppression, in particular for a motor vehicle
2 comprising:
3 - a microphone for registering noises,
4 - a loudspeaker for feeding out acoustic signals for noise suppression,
5 - a circuit arrangement for driving the loudspeaker according to the registered noises
6 which has a drive circuit for provisioning a PWM-modulated clock signal,
7 comprising:
8 - a first input for coupling in an unmodulated first clock signal of a first
9 frequency,
10 - a second input for coupling in a PWM-modulated second clock signal of a
11 second, lower frequency,
12 - a modulator circuit which from the first clock signal generates a PWM-
13 modulated third clock signal of the first frequency which can be tapped at the
14 PWM output of the drive circuit, and
15 - a regulating circuit which regulates the pulse width of the third clock signal
16 until the sum of the pulse duty factors of the second clock signal and of the
17 inverted third clock signal is 100%,
18 and
19 - an output stage which is connected immediately downstream of the drive circuit and
20 which drives the loudspeaker.

1 13. Device according to Claim 12, wherein the output stage is designed as a class
2 D amplifier.

1 14. Device according to Claim 12, wherein the output stage has a driver circuit and
2 a bridge circuit, in particular a full bridge, which is connected downstream of the
3 driver circuit.

- 1 15. Device according to Claim 12, wherein a program-controlled unit, in particular
 - 2 a microcontroller or microprocessor, is provided which is connected immediately
 - 3 upstream of the drive circuit or which has the drive circuit.
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- 1 16. Device according to Claim 12, wherein the output stage is driven directly by a
 - 2 microcontroller.

- 1 17. Method for driving an output stage of a device for noise suppression, in
- 2 particular in a motor vehicle, comprising the steps of:
 - 3 - generating from an unmodulated first clock signal of a first frequency and from a
 - 4 PWM-modulated second clock signal of a second frequency, which is lower than the
 - 5 first frequency, a PWM-modulated third clock signal of the first frequency whose
 - 6 pulse duty factor continues being increased on a regulated basis until the sum of the
 - 7 pulse duty factors of the second clock signal and of the third clock signal is 100%,
 - 8 - using the frequency of the first clock signal as a control variable, and
 - 9 - using the third clock signal made available on the output side as a regulating variable
 - 10 for regulation.
- 1 18. Method according to Claim 17, wherein the first and/or second clock signal
- 2 are/is made available by a program-controlled unit.
- 1 19. Method according to Claim 17, wherein a flip-flop is used for generating the
- 2 pulse width of the PWM-modulated third clock signal.

- 1 20. Use of a microprocessor or microcontroller for directly driving an output stage,
- 2 in particular a class D output stage, with a PWM-modulated clock signal in a device
- 3 for electronic noise suppression.